ABSTRACT

A method and architecture that overcomes the problem of latency-caused performance degradation of electronic memory systems. The method involves a "Posted Precharge," by which an external command for Precharge is given as early as possible, such as immediately following a Read command. The execution of the Precharge is delayed by a precharge counter until all Read/Write commands are completed. By posting a precharge command on a bus at the first available opportunity, multiple pages can be open on the same bank of a memory device. As a result, access latencies are significantly reduced and efficiency of bus in electronic memory systems is significantly improved.